

REMARKS/ARGUMENTS

Applicant received the Office Action dated April 19, 2006 in which the Examiner: 1) rejected claims 1-2 and 4-5 under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent Application Publication No. US 2004/0204096 ("Hirsch"); and 2) rejected claims 3, 6 and 8-21 under 35 U.S.C. § 103(a) as being unpatentable in view of Hirsch and U.S. Patent No. 6,704,584 ("Litwin").

With this Response, Applicant amends claims 1, 5-7, 19 and 21. Based on the amendments and arguments contained herein, Applicant respectfully requests reconsideration and allowance of the pending claims.

§ 102 AND § 103 REJECTIONS

Amended claim 1 recites "the slave device is configurable by the master device to operate in multiple modes including a direct memory addressing mode and an indirect memory addressing mode." None of the references cited by the Examiner, considered individually or together, teach or suggest the above limitation. Hirsch discusses a mode for critical commands that should be completed quickly and a mode for normal commands (see paragraph [0016]) without discussing direct memory addressing and indirect memory addressing. Litwin mentions a read only memory ("ROM") 106 and a random access memory ("RAM") 108, yet also fails to teach or suggest Applicants' claimed "direct memory addressing mode" and "indirect memory addressing mode". For at least these reasons, claim 1 and its dependent claims are allowable over the cited references.

Dependent claim 6 is allowable for the reasons cited above with respect to claim 1. Also, amended claim 6 recites "the master and slave devices selectively switch from the direct memory addressing mode to the indirect memory addressing mode to conserve power." None of the references cited by the Examiner, considered individually or together, teach or suggest this limitation. For at least this additional reason, claim 6 is allowable over the cited references.

With respect to claim 8, the Examiner recognizes that Litwin does not teach "the processor and the slave device are configurable to communicate in multiple modes, each

mode being associated with a different read/write command length", but argues that Hirsch teaches the limitation. Applicant disagrees. Hirsch identifies several ID words, but only one ID word (010) is used for read/write operations. Specifically, ID word 111 indicates a synchronization of the BBDATA signal with the clock BBCLK; ID word 001 indicates a short control word; ID word 010 indicates a long control word that includes address information and a read/write bit; ID word 100 sets the automatic gain control (AGC) loop value; ID word 011 defines the start of a cycle of the AGC loop; and ID word 101 is reserved for future use (see paragraphs [0028]-[0031]). Only ID word 010 is followed by an address and a read/write bit and could be considered by one of ordinary skill in the art to be a read/write command. Since Hirsch teaches only one mode for read/write operations, Hirsch fails to teach "the processor and the slave device are configurable to communicate in multiple modes, each mode being associated with a different read/write command length" as set forth in claim 8. For at least these reasons, claim 8 and its dependent claims are allowable over the cited references.

With respect to claim 13, the Examiner recognizes that Litwin does not teach configuring a device to interpret read/write commands having a non-reduced length and a reduced length, but argues that Hirsch teaches the limitation (see Office action, page 7, item F). As previously described, Hirsch identifies several ID words, but only ID word "010" is followed by an address and a read/write bit and could be considered by one of ordinary skill in the art to be a read/write command. Thus Hirsch does not teach or suggest "configuring a device to interpret read/write commands having a non-reduced length" and "configuring the device to interpret read/write commands having a reduced length if the power consumption parameter exists" as set forth in claim 13.

It is well established that the claimed invention as a whole must be considered (see MPEP 2142.02), yet the Examiner does not appear to address the limitation "configuring the device to interpret read/write commands having a reduced length if the power consumption parameter exists" as set forth in claim 13. In Litwin, a power level is used to determine when a device should relinquish a master device status. Even if Litwin's power level were to be considered a "power consumption parameter" as suggested by the Examiner, relinquishing a master device status based on a power


consumption parameter is simply not the same as "configuring the device to interpret read/write commands having a reduced length if the power consumption parameter exists". None of the references cited by the Examiner, considered individually or together, teach or suggest this limitation. For at least these reasons, claim 13 and its dependent claims are allowable over the cited references.

Amended claim 19, in part, requires "means for configuring the second device in a first mode associated with read/write commands having a non-reduced address field" and "means for configuring the second device in a second mode associated with read/write commands having a reduced address field." As previously described, Hirsch identifies several ID words, but only ID word "010" is followed by an address and a read/write bit and could be considered by one of ordinary skill in the art to be a read/write command. Thus, Hirsch does not teach "read/write commands having a non-reduced address field" and "read/write commands having a reduced address field" as set forth in claim 19. None of the references cited by the Examiner, considered individually or together, teach or suggest the above limitations. For at least this reason, claim 19 and its dependent claims are allowable over the cited references.

CONCLUSION

Applicant respectfully requests reconsideration and that a timely Notice of Allowance be issued in this case. Applicant hereby petitions for any time extensions that are necessary to prevent this case from being abandoned. In the event that additional fees related to this Amendment, or other transactions in this case, are required (including fees for net addition of claims and for time extension), the Examiner is authorized to charge Texas Instruments Inc.'s Deposit Account No. 20-0668 for such fees.

Respectfully submitted,


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AGENT FOR APPLICANT